CLAIMS

What is claimed is:

1. A sensing circuit comprising:

a CMOS inverter amplifier coupled to an input node, said CMOS inverter amplifier for amplifying an input signal;

a resistive feedback circuit coupled to said CMOS inverter amplifier and for cancelling an offset voltage associated with said CMOS inverter amplifier;

a bias circuit coupled to said resistive feedback circuit and for biasing said resistive feedback circuit in a minimally on state to maintain high impedance for said resistive feedback circuit; and

a clamping circuit coupled to said resistive feedback circuit for restricting output swing of an output signal of said CMOS inverter amplifier to maintain said high impedance.

2. The sensing circuit as described in Claim 1, wherein said input signal is a capacitively coupled differential clock signal from a vernier structure.

3. The sensing circuit as described in Claim 2, wherein said differential clock signal is a 3.3 volt clock signal coupled through a minimum of 0.1fF differential coupling capacitance and having a frequency of between 0-20 MHz.

4. The sensing circuit as described in Claim 1, wherein said resistive feedback circuit biases said CMOS inverter amplifier to a threshold voltage associated with said CMOS inverter amplifier to cancel said offset voltage.

5. The sensing circuit as described in Claim 1, wherein said resistive feedback circuit comprises:

a PMOS transistor comprising a PMOS source coupled to an output of said CMOS inverter amplifier that provides said output signal, a PMOS gate, and a PMOS drain coupled to said input node; and

an NMOS transistor comprising an NMOS drain coupled to said PMOS source, an NMOS gate, and an NMOS source coupled to said output.

6. The sensing circuit as described in Claim 1, wherein said bias circuit comprises:

a second CMOS inverter amplifier of similar dimension to said CMOS inverter amplifier, said second CMOS inverter amplifier comprising a PMOS transistor and an NMOS transistor in a standard inverter configuration; and

an NMOS diode coupled in series between said PMOS transistor and said NMOS transistor, said NMOS diode for providing a p-bias voltage from said PMOS transistor to said resistive feedback circuit that is slightly lower than a threshold voltage associated with said CMOS inverter

amplifier, and an n-bias voltage from said NMOS transistor that is slightly higher than said threshold voltage.

7. The sensing circuit as described in Claim 1, wherein said clamp circuit comprises:

a PMOS transistor comprising a PMOS source coupled to an output of said CMOS inverter amplifier that provides said output signal, a PMOS gate coupled to a first bias voltage slightly lower than a threshold voltage of said CMOS inverter amplifier, and a PMOS drain coupled to a bias node;

said bias node;

an NMOS transistor comprising an NMOS drain coupled to bias node, an NMOS gate coupled to a second bias voltage slightly higher than said threshold voltage, and an NMOS source coupled to said output; and

a second CMOS inverter amplifier of similar dimension to said CMOS inverter amplifier, and comprising a second input coupled to said bias node and a second output coupled to said bias node.

8. The sensing circuit as described in Claim 1, wherein said CMOS inverter amplifier is a first amplification stage, and further comprising:

a second amplification stage comprising a second CMOS inverter amplifier coupled to said output, said second CMOS inverter amplifier of similar dimension and configuration as said CMOS inverter amplifier; and

a third amplification stage comprising a third CMOS inverter amplifier coupled to said second CMOS inverter amplifier.

9. A low frequency sensing circuit comprising:

a CMOS inverter amplifier for amplifying an input signal and comprising an output coupled to a mid node, said CMOS inverter amplifier associated with a threshold voltage; and

a resistive feedback circuit for biasing said CMOS inverter amplifier at said threshold voltage and cancelling an offset voltage associated with said CMOS inverter amplifier, and comprising:

a PMOS transistor operating in a subthreshold conduction region comprising a PMOS source coupled to said mid node, a PMOS drain coupled to an input node of said CMOS inverter amplifier, and a PMOS gate coupled to a first bias voltage that is slightly below said threshold voltage; and

an NMOS transistor operating in said subthreshold conduction region comprising an NMOS drain coupled to said input node, an NMOS source coupled to said mid node; and an NMOS gate coupled to a second bias voltage that is slightly above said threshold voltage.

10. The sensing circuit as described in Claim 9, wherein said CMOS inverter amplifier comprises:

a second PMOS transistor; and

a second NMOS transistor coupled to said second PMOS transistor in a standard CMOS inverter configuration, wherein said CMOS inverter amplifier is coupled to a ground and a supply voltage V_{dd}, such that an output signal present at said output swings from ground to said V_{dd}.

11. The sensing circuit as described in Claim 9, further comprising a bias circuit for biasing said resistive feedback circuit, and comprising:

a second PMOS transistor comprising a second PMOS source coupled to a supply voltage, a second PMOS gate, and a second PMOS drain coupled to said second PMOS gate, said second PMOS drain providing said second bias voltage;

an NMOS diode comprising a diode drain coupled to said second PMOS drain, a diode gate coupled to said diode drain, and a diode source; and

a second NMOS transistor comprising a second NMOS drain coupled to said diode source, a second NMOS gate coupled to said second NMOS drain, and a second NMOS source coupled to ground, said second NMOS drain providing said first bias voltage.

12. The sensing circuit as described in Claim 9, further comprising a clamping circuit for restricting an output swing of said CMOS inverter amplifier, and comprising:

a second PMOS transistor comprising a second PMOS source coupled to said mid node a second PMOS gate coupled to

said first bias voltage and a second PMOS drain coupled to a second mid node;

a second NMOS transistor comprising a second NMOS drain coupled to said second mid node, a second NMOS gate coupled to said second bias voltage, and a second NMOS source coupled to said mid node; and

a second CMOS inverter amplifier of similar dimension and configuration as said CMOS inverter amplifier for reducing a gain of said CMOS inverter amplifier to restrict said output swing.

13. The sensing circuit as described in Claim 12, wherein said second PMOS transistor is substantially larger than a third PMOS transistor in said resistive feedback circuit, and wherein said second NMOS transistor is substantially larger than a third PMOS transistor in said resistive feedback circuit.

14. The sensing circuit as described in Claim 9, wherein said CMOS inverter amplifier is a first amplification stage, and further comprising:

a second amplification stage comprising a second CMOS inverter amplifier coupled to said output, said second CMOS inverter amplifier of similar dimension and configuration as said CMOS inverter amplifier; and

a third amplification stage comprising a third CMOS inverter amplifier coupled to said second CMOS inverter amplifier.

15. The sensing circuit as described in Claim 9, wherein said resistive feedback circuit exhibits low parasitic capacitance to reduce effect on said input signal, and presents a high impedance at said input node to allow said CMOS inverter amplifier to amplify signals below 20 MHz.

16. The sensing circuit as described in Claim 9, wherein said input signal is a capacitively coupled differential clock signal from a vernier structure.

17. The sensing circuit as described in Claim 9, wherein said threshold voltage is one half of a supply voltage V_{dd} that is supplied to said CMOS inverter amplifier.

18. A method for cancelling offset voltage in a sensing circuit comprising:

a) amplifying an input signal to said sensing circuit with a CMOS inverter amplifier;

b) biasing said CMOS inverter amplifier to a threshold voltage associated with said CMOS inverter amplifier to cancel an offset voltage associated with said CMOS inverter amplifier;

c) maintaining a high input impedance at said input signal to amplify low frequency signals up to 20 MHz by operating MOSFET transistors of said resistive feedback circuit in a MOSFET subthreshold conduction region; and

d) clamping an output swing of an output signal of said CMOS inverter amplifier to maintain said high input impedance.

19. The method as described in Claim 18, further comprising:

performing a second amplification by amplifying said output signal with a second CMOS inverter amplifier substantially similar in dimension and configuration as said CMOS inverter amplifier.

20. The method as described in Claim 19, further comprising:

performing a third stage amplification by amplifying a second output signal from said second CMOS inverter amplifier to bring said second output signal up to a full swing digital output voltage for frequencies below 1 MHz of said input signal.

21. The method as described in Claim 18, wherein b) further comprises feeding said output signal of said CMOS inverter amplifier through a resistive feedback circuit and back to said input node.

22. The method as described in Claim 18, wherein c) further comprises:

c1) closely replicating said CMOS inverter amplifier in a bias circuit comprising a PMOS transistor and an NMOS transistor; and

c2) coupling an NMOS diode in series to said PMOS transistor and said NMOS transistor for providing a first bias voltage from said PMOS transistor to said resistive feedback circuit that is slightly below said threshold voltage, and for providing a second bias voltage from said NMOS transistor to said resistive feedback circuit that is slightly above said threshold voltage.

23. The method as described in Claim 22, wherein said PMOS transistor is slightly smaller than a second PMOS transistor in said CMOS inverter amplifier; and

wherein said NMOS transistor is slightly larger than a second NMOS transistor in said CMOS inverter amplifier.

24. The method as described in Claim 18, wherein d) further comprises:

restricting said output swing by coupling a PMOS and NMOS switch transistors that are substantially larger than MOSFET transistors in said resistive feedback circuit, and switching said PMOS and NMOS switch transistors on when said output voltage swings too high; and

coupling a second CMOS inverter amplifier to said PMOS and NMOS switch transistors to attenuate gain from said CMOS inverter amplifier when said PMOS and NMOS switch transistors are turned on.

25. A vernier alignment structure comprising a receiver comprising a plurality of sensing circuits, each for generating an alignment signal, and comprising:

a CMOS inverter amplifier coupled to an input node, said CMOS inverter amplifier for amplifying an input signal;

a resistive feedback circuit coupled to said CMOS inverter amplifier and for cancelling an offset voltage associated with said CMOS inverter amplifier; and

a bias circuit coupled to said resistive feedback circuit and for biasing said resistive feedback circuit in a minimally on state to maintain high impedance for said resistive feedback circuit.

26. The vernier alignment structure as described in Claim 25, wherein said input signal is a capacitively coupled differential clock signal.

27. The vernier alignment structure as described in Claim 26, wherein said differential clock signal is a 3.3 volt clock signal coupled through a minimum of 0.1fF differential coupling capacitance and having a frequency of between 0-20 MHz.

28. The vernier alignment structure as described in Claim 25, wherein said resistive feedback circuit biases said CMOS inverter amplifier to a threshold voltage associated with said CMOS inverter amplifier to cancel said offset voltage.

29. The vernier alignment structure as described in Claim 25, wherein said resistive feedback circuit comprises:

a PMOS transistor comprising a PMOS source coupled to an output of said CMOS inverter amplifier that provides said output signal, a PMOS gate, and a PMOS drain coupled to said input node; and

an NMOS transistor comprising an NMOS drain coupled to said PMOS source, an NMOS gate, and an NMOS source coupled to said output.

30. The vernier alignment structure as described in Claim 25, wherein said bias circuit comprises:

a second CMOS inverter amplifier of similar dimension to said CMOS inverter amplifier, said second CMOS inverter amplifier comprising a PMOS transistor and an NMOS transistor in a standard inverter configuration; and

an NMOS diode coupled in series between said PMOS transistor and said NMOS transistor, said NMOS diode for providing a p-bias voltage from said PMOS transistor to said resistive feedback circuit that is slightly lower than a

threshold voltage associated with said CMOS inverter amplifier, and an n-bias voltage from said NMOS transistor that is slightly higher than said threshold voltage.

31. The vernier alignment structure as described in Claim 25, further comprising a clamping circuit coupled to said resistive feedback circuit for restricting output swing of an output signal of said CMOS inverter amplifier to maintain said high impedance.

32. The vernier alignment structure as described in Claim 31, wherein said clamping circuit comprises:

a PMOS transistor comprising a PMOS source coupled to an output of said CMOS inverter amplifier that provides said output signal, a PMOS gate coupled to a first bias voltage slightly lower than a threshold voltage of said CMOS inverter amplifier, and a PMOS drain coupled to a bias node;

said bias node;

an NMOS transistor comprising an NMOS drain coupled to bias node, an NMOS gate coupled to a second bias voltage slightly higher than said threshold voltage, and an NMOS source coupled to said output; and

a second CMOS inverter amplifier of similar dimension to said CMOS inverter amplifier, and comprising a second input coupled to said bias node and a second output coupled to said bias node.

33. The sensing circuit as described in Claim 25, wherein said CMOS inverter amplifier is a first amplification stage, and further comprising:

a second amplification stage comprising a second CMOS inverter amplifier coupled to said output, said second CMOS inverter amplifier of similar dimension and configuration as said CMOS inverter amplifier; and

a third amplification stage comprising a third CMOS inverter amplifier coupled to said second CMOS inverter amplifier.

34. A vernier alignment structure for measuring distance comprising:

a transmitter chip comprising a plurality of transmitter pads spaced along a first line at a pitch of x, said transmitter chip actively driving complementary waveforms from an input signal in an alternating pattern over said plurality of transmitter pads;

a receiving chip comprising a plurality of receiving pads spaced along a second line at a pitch of y, said first line in parallel with said second line and separated by a distance; and

a plurality of sensing circuits coupled to said plurality of receiving pads, said plurality of sensing circuits able to measure a change in said distance through capacitive coupling between said plurality of transmitting pads and said plurality of receiving pads.

35. The vernier alignment structure as described in Claim 34, wherein at least one of said plurality of sensing circuits comprises:

a CMOS inverter amplifier coupled to an input node, said CMOS inverter amplifier for amplifying a second input signal from an associated receiving pad;

a resistive feedback circuit coupled to said CMOS inverter amplifier and for cancelling an offset voltage associated with said CMOS inverter amplifier;

a bias circuit coupled to said resistive feedback circuit and for biasing said resistive feedback circuit in a minimally on state to maintain high impedance for said resistive feedback circuit; and

a clamping circuit coupled to said resistive feedback circuit for restricting output swing of an output signal of said CMOS inverter amplifier to maintain said high impedance.

36. The vernier alignment structure as described in Claim 34, wherein said plurality of sensing circuit are able to measure said distance.

37. The vernier alignment structure as described in Claim 34, wherein said input signal is a clock signal.